In the Specification:

Please replace the paragraph beginning on page 15 line 19 with the following amended paragraph:

Host 24 and HCA 22 are connected by a suitable system controller 28 to a system memory 32 via a bus 30, such as a Peripheral Component Interface (PCI) bus, as is known in the art. The HCA and memory typically occupy certain ranges of physical addresses in a defined address space on the bus. In order to send and receive packets over fabric 26, consumer processes on host 24 write descriptors 34 to memory 32. Descriptors 34 are preferably prepared and executed in the form of a linked list, as described in U.S. ~~patent application Ser. No. 09/870,016, filed May 31, 2001,~~ Patent No. 6,735,642, issued May 11, 2004, which is assigned to the assignee of the present patent application, and whose disclosure is incorporated herein by reference. A separate linked list of descriptors is preferably maintained for each QP in use by host 24.